Remarks

Applicants thank the Examiner for his careful consideration of this application. Reconsideration of this application is now respectfully requested in view of the amendments above and the following remarks.

Claims 1 and 3-18 are now pending in the application, with Claims 1, 3, 11, and 16-18 being the independent claims.

Applicants acknowledge with gratitude the withdrawal of the double-patenting rejections found in the previous Office Action, in view of the Terminal Disclaimer filed by Applicants with their response of June 10, 2005.

At pages 2, the Office Action objects to the abstract. In response, Applicants submit herewith a new abstract, on a separate sheet. Applicants request withdrawal of this objection in view of the new abstract.

At pages 2-4, the Office Action rejects Claims 1, 3-5, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy (U.S. Patent No. 5,994,766) in view of Sivilotti et al. (U.S. Patent No. 6,316,334). At page 4, the Office Action rejects Claims 6-8 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy and Sivilotti et al., further in view of IBM Technical Disclosure Bulletin 6/86, Vol. 29, No. 1, pp. 88-94 ("TDB") and Cox. Finally, at pages 4-6, the Office Action rejects Claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Shenoy,

Sivilotti et al. and TDB or Cox, and further in view of Hively. These rejections are respectfully traversed for at least the following reasons.

Applicants maintain that the combination of Shenoy et al. and Sivilotti et al. is not technically possible and that it fails to teach or suggest all elements of the claimed invention. There are a number of reasons for these assertions.

First, Applicants maintain that, in connection with Claims 1 and 18, as well as in Claims 3, 16, and 17 (as well as the claims depending from these claims), there is no logic array in Shenoy et al., and furthermore, that there is no repeating core in Shenoy et al.

The Office Action at page 7 asserts that Shenoy et al. at col. 4, col. 66 to col. 5, line 5 contains such teachings. However, Applicants note that the only repeating elements discussed in this portion of Shenoy et al. is "one or more input/output (I/O) ports, which may be considered to include any input/output buffers, pads, terminals, etc.[,] defined in the logic circuit for the purpose of communicating a signal between the logic circuit and an external device," which "are typically arranged in linear arrays." Shenoy et al., col. 5, lines 1-10. Thus, Shenoy et al. describes an array of I/O ports, but **not a *logic* array**.

Additionally, given that Shenoy et al. does not deal with a logic array, there is no motivation for one of ordinary skill in the art to employ a borderless logic array, as asserted at page 3.

Next, it is further submitted that the cited prior art fails to teach or suggest configurable I/Os, as found in Claims 1, 11, and 18 (and their dependent claims) In connection with this,

Applicants maintain their previous arguments in connection with Claims 1 and 11 (and their dependent claims), which also apply to Claim 18. These arguments are repeated below, for the convenience of the reader. Applicants have also added some additional material to these arguments to bolster and clarify these arguments.

First, Applicants argue that "configurable I/O" is not stated as an "intended use," as discussed at page 6, but rather, it is found as a structural limitation in the claims in which it appears. Therefore, the fact that it is not taught in or suggested by Shenoy et al. or Sivilotti et al. means that this limitation has not been taught or suggested by the prior art, and therefore, there is no *prima facie* case of obviousness because when they are combined, there is still at least one element (configurable I/O) that is not taught or suggested.

Next, Claims 1 and 11 (as previously amended) and Claim 18 all recite the presence of "configurable I/O cells." This term appears in the specification, for example, in paragraphs 129, 154, and 158. In particular, paragraph 129 discusses a "configurable I/O that could be customized to the specific function by the customized layers." Paragraph 154 discusses "via-configurable I/O." Paragraph 158 discusses "enhanced via-configurable I/O." Note that element 26 in Fig. 2 is described in the specification (e.g., in paragraph 157) as being an "I/O cell" and is also referred to (e.g., in paragraph 129) as being an "area I/O." Hence, it is clear that the terms "I/O cell" and "area I/O" are being used interchangeably, and that all of these portions of the specification are discussing the same thing.

Given this, it becomes clear that "configurable I/O cells" are I/O cells that may be customized to perform particular functions (which may include, but are not limited to, input, output, differential input, differential output, and/or other functions). This may be done by designing customized layers or by the use of vias to make various connections (or, the vias may be included in a customized via layer).

With this understanding of what is meant by "configurable I/O cells," a careful perusal of Shenoy et al. and Sivilotti et al. reveals that neither of these references discloses or suggests the use of configurable I/O cells. In particular, the Office Action relies on Shenoy et al. at Fig. 1 and col. 4, line 66 to col. 5, line 11 to teach the use of configurable I/O cells. Applicants, however, are able to find no such teaching there or anywhere else in Shenoy et al. (or anywhere in Sivilotti et al.). On the contrary, Applicants note that Shenoy et al. only teaches I/Os "that may be considered to include any input/output buffers, pads, terminals, etc.[,] defined in the logic circuit for the purpose of communicating a signal between the logic circuit and an external device" and "that are typically arranged in linear arrays of cells or tiles along the periphery of an integrated circuit device." Shenoy et al., col. 5, lines 3-6 and 10-12. There is no discussion of any characteristics of the I/Os as being "configurable" (or anything that might be considered synonymous with "configurable") in Shenoy et al. For at least these reasons, therefore, it is respectfully submitted that Claims 1, 11-14, and 18 are allowable over the cited prior art.

It is further noted that Shenoy et al. teaches the use of "fixed potential shield traces between pairs of non-differential signal traces to reduce capacitative coupling between the signal

traces." Shenoy et al., col. 4, lines 3-6. Shenoy et al. goes on to teach that "[f]or differential pairs of signal traces which cooperatively carry a differential signal, shield traces are not utilized between the signal traces in a differential pair, since it is not problematic, and it can often be beneficial, for coupling to exist between the signal traces in a differential pair." This appears to teach that I/Os are defined as being part of a differential pair or a non-differential pair and thus are not configurable.

Furthermore, in connection with Claims 3-10, 16, and 17, Applicants respectfully submit that Sivilotti et al. describes a continuous array utilizing repeating blocks of transistors 22, as shown in Fig. 3 and described at col. 3, lines 12-21. Once a desired size for a device is defined, then another block 22c may be unused, and another block 22b may be connected to a utilized block 22a to support I/O functionality. Therefore, there is no need for the use of a redistribution layer, as in Shenoy et al. or in any other prior art reference. Hence, one of ordinary skill in the art would not have been motivated to combine Shenoy et al., or any other reference teaching a redistribution layer for redistribution of I/O, with the teachings of Sivilotti et al. Furthermore, in connection with all claims, this provides a general reason why one of ordinary skill in the art would *not* combine these two references.

Also dictating against the combination of Shenoy et al. with Sivilotti et al. is the fact that Shenoy et al. discusses that "I/O ports are disposed within I/O 'slots'," at col. 5, line 7. In contrast, Sivilotti et al. permits the use of any portion of a regular circuit fabric to be connected to an I/O pad, as discussed, e.g., at col. 3, lines 31-35.

Furthermore, Claims 1 and 16-18 (and their dependent claims) specifically recite the use of "area I/O." Shenoy et al., as discussed above, teaches that "I/O ports are disposed within I/O 'slots'" that are typically arranged in linear arrays "**along the periphery of an integrated circuit device**." Shenoy et al., col. 5, lines 7 and 10-12. Furthermore, the various figures of Shenoy et al. show the I/O ports located peripherally. Additionally, the focus of Sivilotti et al., noting, for example, Figs. 1 and 3, and associated discussion in col. 3, lines 26-34, is on constructing peripheral I/O (i.e., on the periphery of a particular device). In contrast, Applicant's claimed area I/Os, note, e.g., paragraphs 129-132 and Figs. 2-1 and 3C, while located at the periphery of are connected to provide I/O to various devices on various areas of the overall device, rather than at the periphery of a particular device. This has the advantage of providing greater design flexibility.

Claim 1 and its dependent claim (Claim 14) and Claim 18 recite that the "configurable I/O comprises at least one metal layer that is the same for all I/O configurations." The Office Action asserts, e.g., at page 3, that "[t]he use of [] at least one metal which is the same for all I/O configuration [*sic*] would have been obvious corresponding to the processing step as opposed to a structural difference." Applicants respectfully submit that this is a structural limitation and that it is not obvious to combine it, e.g., with Sivilotti et al. To wit, Sivilotti et al. would not be operative with one metal layer that is the same for all I/Os. This is evident from examination of Fig. 3 and its corresponding discussion (col. 3, lines 12 ff.). For example, in the area marked with reference numeral 22c, there is no metal, while in the area marked with reference numeral

22b, there is flat metal used for pad 32, while in the area marked with reference numeral 22a, there is metal connectivity as needed to create the necessary logic and I/O structure. It is also noted that Shenoy et al. fails to teach the use of a same metal layer for all I/O configurations, as Shenoy et al. fails to discuss any specific I/O structure. Hence, neither of the cited references, teaches or suggests such a metal layer, and the use of such a metal layer would render Sivilotti et al. inoperable as disclosed. Therefore, one of ordinary skill in the art would not have considered it obvious to use a metal layer that is the same for all I/Os.

The Office Action goes on to assert that a further reason why it would have been obvious to use a same metal layer for all I/Os is that "the same metal layer can be patterned in the same step or using the same masking, as opposed to using different metal layer [*sic*] for different I/O," citing Sivilotti et al. at col. 3, lines 53-62. However, it is noted that Sivilotti et al. did not teach the use of a single metal layer as a solution to any stated problem. In contrast, as discussed at col. 3, line 59 to col. 4, line 3, Sivilotti et al. proposed to

> plac[e] all of the patterns A1, A2 and A3 (or, for example A1 through A3 and B1 through B6 for a multi-project wafer) onto a single mask 62a or 62b (Figs. 7a and 7b), appropriately aligning the mask for each layer, and then blocking off all but the desired pattern with an opaque cover 64 (Fig. 8) so that only the desired pattern is exposed.

Sivilotti et al. goes on to note that "[t]he exposure in this approach must, of course, be carefully controlled." Sivilotti et al., col. 4, lines 3-4. This is not, however, using a

common pattern on multiple designs; this is using different patterns for different designs and results in additional complexity (one reason being that, as Sivilotti et al. states, the exposure must be carefully controlled, another being that this may result in propagation of defects). In short, Sivilotti's approach was to put different metal patterns on a single mask but to expose only a portion of a single mask each time (which is a far more complex operation than using the same mask for different designs). While Sivilotti et al., indeed, recognizes that masks are expensive, this reference states an entirely different solution to an entirely different problem from that being addressed by the presently claimed invention.

While Applicants do not necessarily concur with the Office Action's characterizations of the claims and/or the references with regard to other claimed features, Applicants choose not to discuss each such feature. Consequently, the lack of explicit discussion is not to be understood as indicating tacit agreement with such characterizations.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants, therefore, respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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